What is claimed is:

1. A computer implemented method for functionally abstracting a memory column, comprising:

identifying, in a description of a circuit, at least one column of n memory cells, where n is an integer greater than 1;

representing said column of n memory cells as a single-memory-cell column comprising a single representative memory cell;

abstracting at least a portion of said single-memory-cell column to derive a logic-level representation for said representative memory cell; and

generating one or more additional instances of said logic-level representation to derive an abstracted memory column comprising a plurality of instances of said logic-level representation.

2. The method of claim 1, wherein said logic-level representation comprises a latch.

3. The method of claim 2, wherein generating one or more additional instances comprises:

generating n-1 additional instances of said logic-level representation to derive an abstracted memory column comprising n instances of said logic-level representation.

4. The method of claim 1, wherein abstracting comprises:

deriving a gate-level representation for said representative memory cell; and

abstracting a latch from at least a portion of said gate-level representation.

5. The method of claim 4, wherein deriving a gate-level representation comprises:

applying symbolic analysis to a transistor level description of said representative memory cell.

6. The method of claim 1, wherein identifying a column of n memory cells comprises:

verifying that all of said n memory cells are substantially identical in structure relative to each other.

7. The method of claim 6, further comprising:

selecting one of said n memory cells to be said representative memory cell.

8. The method of claim 7, wherein representing said column of n memory cells as a single-memory-cell column comprises:

removing all of said n memory cells except for said representative memory cell from said column.

9. The method of claim 1, wherein said representative memory cell is initially coupled to a particular select line, and wherein representing said column of n memory cells as a single-memory-cell column comprises:

decoupling said representative memory cell from said particular select line.

10. The method of claim 9, wherein abstracting said single-memory-cell column comprises:

coupling said logic-level representation of said representative memory cell to said particular select line.

11. The method of claim 1, wherein generating additional instances of said logic-level representation comprises:

generating one or more additional instances of said logic-level representation; and

for each additional instance generated, coupling that instance to a distinct select line.

12. The method of claim 11, wherein generating additional instances of said logic-level representation further comprises:

making an explicit assumption that selection of each select line is mutually exclusive relative to all other select lines.

13. The method of claim 1, wherein said abstracted memory column is cycle ready.

14. An apparatus for functionally abstracting a memory column, comprising:

a mechanism for identifying, in a description of a circuit, at least one column of n memory cells, where n is an integer greater than 1;

a mechanism for representing said column of n memory cells as a single-memory-cell column comprising a single representative memory cell;

a mechanism for abstracting at least a portion of said single-memory-cell column to derive a logic-level representation for said representative memory cell; and

a mechanism for generating one or more additional instances of said logic-level representation to derive an abstracted memory column comprising a plurality of instances of said logic-level representation.

15. The apparatus of claim 14, wherein said logic-level representation comprises a latch.

16. The apparatus of claim 15, wherein the mechanism for generating one or more additional instances comprises:

a mechanism for generating n-1 additional instances of said logic-level representation to derive an abstracted memory column comprising n instances of said logic-level representation.

17. The apparatus of claim 14, wherein the mechanism for abstracting comprises:

a mechanism for deriving a gate-level representation for said representative memory cell; and

a mechanism for abstracting a latch from at least a portion of said gate-level representation.

18. The apparatus of claim 17, wherein the mechanism for deriving a gate-level representation comprises:

a mechanism for applying symbolic analysis to a transistor level description of said representative memory cell.

19. The apparatus of claim 14, wherein the mechanism for identifying a column of n memory cells comprises:

a mechanism for verifying that all of said n memory cells are substantially identical in structure relative to each other.

20. The apparatus of claim 19, further comprising:

a mechanism for selecting one of said n memory cells to be said representative memory cell.

21. The apparatus of claim 20, wherein the mechanism for representing said column of n memory cells as a single-memory-cell column comprises:

a mechanism for removing all of said n memory cells except for said representative memory cell from said column.

22. The apparatus of claim 14, wherein said representative memory cell is initially coupled to a particular select line, and wherein the mechanism for representing said column of n memory cells as a single-memory-cell column comprises:

a mechanism for decoupling said representative memory cell from said particular select line.

23. The apparatus of claim 22, wherein the mechanism for abstracting said single-memory-cell column comprises:

a mechanism for coupling said logic-level representation of said representative memory cell to said particular select line.

24. The apparatus of claim 14, wherein the mechanism for generating additional instances of said logic-level representation comprises:

a mechanism for generating one or more additional instances of said logic-level representation; and

a mechanism for coupling, for each additional instance generated, that instance to a distinct select line.

25. The apparatus of claim 24, wherein the mechanism for generating additional instances of said logic-level representation further comprises:

a mechanism for making an explicit assumption that selection of each select line is mutually exclusive relative to all other select lines.

26. The apparatus of claim 14, wherein said abstracted memory column is cycle ready.

27. A computer readable medium, comprising:

instructions for causing one or more processors to identify, in a description of a circuit, at least one column of n memory cells, where n is an integer greater than 1;

instructions for causing one or more processors to represent said column of n memory cells as a single-memory-cell column comprising a single representative memory cell;

instructions for causing one or more processors to abstract at least a portion of said single-memory-cell column to derive a logic-level representation for said representative memory cell; and

instructions for causing one or more processors to generate one or more additional instances of said logic-level representation to derive an abstracted memory column comprising a plurality of instances of said logic-level representation.

28. The computer readable medium of claim 27, wherein said logic-level representation comprises a latch.

29. The computer readable medium of claim 28, wherein the instructions for causing one or more processors to generate one or more additional instances comprises:

instructions for causing one or more processors to generate n-1 additional instances of said logic-level representation to derive an abstracted memory column comprising n instances of said logic-level representation.

30. The computer readable medium of claim 27, wherein the instructions for causing one or more processors to abstract comprises:

instructions for causing one or more processors to derive a gate-level representation for said representative memory cell; and

instructions for causing one or more processors to abstract a latch from at least a portion of said gate-level representation.

31. The computer readable medium of claim 30, wherein the instructions for causing one or more processors to derive a gate-level representation comprises:

instructions for causing one or more processors to apply symbolic analysis to a transistor level description of said representative memory cell.

32. The computer readable medium of claim 27, wherein the instructions for causing one or more processors to identify a column of n memory cells comprises:

instructions for causing one or more processors to verify that all of said n memory cells are substantially identical in structure relative to each other.

33. The computer readable medium of claim 32, further comprising:

instructions for causing one or more processors to select one of said n memory cells to be said representative memory cell.

34. The computer readable medium of claim 33, wherein the instructions for causing one or more processors to represent said column of n memory cells as a single-memory-cell column comprises:

instructions for causing one or more processors to remove all of said n memory cells except for said representative memory cell from said column.

35. The computer readable medium of claim 27, wherein said representative memory cell is initially coupled to a particular select line, and wherein the instructions for causing one or more processors to represent said column of n memory cells as a single-memory-cell column comprises:

instructions for causing one or more processors to decouple said representative memory cell from said particular select line.

36. The computer readable medium of claim 35, wherein the instructions for causing one or more processors to abstract said single-memory-cell column comprises:

instructions for causing one or more processors to couple said logic-level representation of said representative memory cell to said particular select line.

37. The computer readable medium of claim 27, wherein the instructions for causing one or more processors to generate additional instances of said logic-level representation comprises:

instructions for causing one or more processors to generate one or more additional instances of said logic-level representation; and

instructions for causing one or more processors to couple, for each additional instance generated, that instance to a distinct select line.

38. The computer readable medium of claim 37, wherein the instructions for causing one or more processors to generate additional instances of said logic-level representation further comprises:

instructions for causing one or more processors to make an explicit assumption that selection of each select line is mutually exclusive relative to all other select lines.

39. The computer readable medium of claim 27, wherein said abstracted memory column is cycle ready.